

INTERNATIONAL STANDARD

**Qi Specification version 2.0 –
Part 4: Power Delivery**

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QI SPECIFICATION VERSION 2.0 –

Part 4: Power Delivery

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It is based on *Qi Specification version 2.0, Power Delivery* and was submitted as a Fast-Track document.

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Draft	Report on voting
100/4249/FDIS	100/4279/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

The structure and editorial rules used in this publication reflect the practice of the organization which submitted it.

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Qi Specification

Power Delivery

Version 2.0

April 2023

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RELEASE HISTORY

Specification Version	Release Date	Description
2.0	April 2023	Initial release of the v2.0 Qi Specification.

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Table of Contents

1 General	3
1.1 Structure of the Qi Specification	3
1.2 Scope	4
1.3 Compliance	4
1.4 References	4
1.5 Conventions	5
1.6 Power Profiles	7
2 Introduction	8
3 Power Receiver construction	10
3.1 Dual resonant circuit	13
3.2 Rectification circuit	15
3.3 Sensing circuits	15
3.4 Communications modulator	15
3.5 Communications demodulator	15
3.6 Output disconnect	15
3.7 Shielding	16
4 Power Receiver design guidelines (informative)	17
4.1 Large-signal resonance check	17
4.2 Power Receiver coil design	18
5 Power Transmitter construction	19
5.1 Power Transmitter reference designs	19
5.2 Power transfer control	19
6 Power consumption	22
7 Meaningful functionality	23
8 Unintentional Magnetic Field Susceptibility (Informative)	24
8.1 Limits	24
8.2 Protection	24
8.3 Power Transmitter detection	24
9 Load Steps	25
9.1 Load step test procedure	25
9.2 Load dump test procedure	28

10 Over-voltage protection	30
11 External Power Input (Informative)	37
11.1 Available power—Extended Power Profile only	37
12 Power Levels (Extended Power Profile only)	38
12.1 Potential Load Power	38
12.2 Light load	38
13 System Efficiency (Informative)	39
13.1 Definition	39
13.2 Power Transmitter efficiency	40
13.3 Power Receiver efficiency	42
14 Stand-by Power (Informative)	43
14.1 Transmitter Measurement Method	43
15 Object Detection (Informative)	44
15.1 Resonance shift	44
15.2 Capacitance change	46
16 Power Receiver Localization (Informative)	47
16.1 Primary Coil array based Free Positioning	47
16.2 Moving Primary Coil based Free Positioning	50
16.3 User-assisted positioning	51

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1 General

The Wireless Power Consortium (WPC) is a worldwide organization that aims to develop and promote global standards for wireless power transfer in various application areas. A first application area comprises flat-surface devices such as mobile phones and chargers in the Baseline Power Profile (up to 5 W) and Extended Power Profile (above 5 W).

1.1 Structure of the Qi Specification

General documents

- Introduction
- Glossary, Acronyms, and Symbols

System description documents

- Mechanical, Thermal, and User Interface
- Power Delivery
- Communications Physical Layer
- Communications Protocol
- Foreign Object Detection
- NFC Tag Protection
- Authentication Protocol

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1.2 Scope

The *Qi Specification, Power Delivery* (this document) comprises guidelines and requirements for Power Receiver design, including circuitry, power consumption, operating power levels, power transfer efficiency, and standby power.

1.3 Compliance

All provisions in the *Qi Specification* are mandatory, unless specifically indicated as recommended, optional, note, example, or informative. Verbal expression of provisions in this Specification follow the rules provided in ISO/IEC Directives, Part 2.

Table 1: Verbal forms for expressions of provisions

Provision	Verbal form
requirement	“shall” or “shall not”
recommendation	“should” or “should not”
permission	“may” or “may not”
capability	“can” or “cannot”

1.4 References

For undated references, the most recently published document applies. The most recent WPC publications can be downloaded from <http://www.wirelesspowerconsortium.com>.

1.5 Conventions

1.5.1 Notation of numbers

- Real numbers use the digits 0 to 9, a decimal point, and optionally an exponential part.
- Integer numbers in decimal notation use the digits 0 to 9.
- Integer numbers in hexadecimal notation use the hexadecimal digits 0 to 9 and A to F, and are prefixed by "0x" unless explicitly indicated otherwise.
- Single bit values use the words ZERO and ONE.

1.5.2 Tolerances

Unless indicated otherwise, all numeric values in the *Qi Specification* are exactly as specified and do not have any implied tolerance.

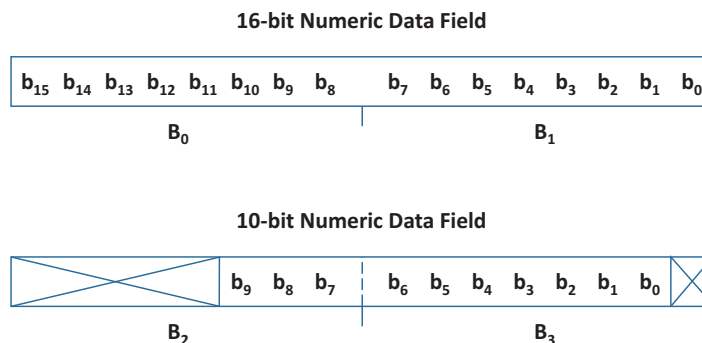
1.5.3 Fields in a data packet

A numeric value stored in a field of a data packet uses a big-endian format. Bits that are more significant are stored at a lower byte offset than bits that are less significant. [Table 2](#) and [Figure 1](#) provide examples of the interpretation of such fields.

Table 2: Example of fields in a data packet

	b₇	b₆	b₅	b₄	b₃	b₂	b₁	b₀
B₀	(msb) 16-bit Numeric Data Field (lsb)							
B₁								
B₂	Other Field					(msb)		
B₃	10-bit Numeric Data Field						(lsb)	Field

Figure 1. Examples of fields in a data packet



1.5.4 Notation of text strings

Text strings consist of a sequence of printable ASCII characters (i.e. in the range of 0x20 to 0x7E) enclosed in double quotes ("). Text strings are stored in fields of data structures with the first character of the string at the lowest byte offset, and are padded with ASCII NUL (0x00) characters to the end of the field where necessary.

EXAMPLE: The text string "WPC" is stored in a six-byte field as the sequence of characters 'W', 'P', 'C', NUL, NUL, and NUL. The text string "M:4D3A" is stored in a six-byte field as the sequence 'M', ':', '4', 'D', '3', and 'A'.

1.5.5 Short-hand notation for data packets

In many instances, the *Qi Specification* refers to a data packet using the following shorthand notation:

<MNEMONIC>/<modifier>

In this notation, <MNEMONIC> refers to the data packet's mnemonic defined in the *Qi Specification, Communications Protocol*, and <modifier> refers to a particular value in a field of the data packet. The definitions of the data packets in the *Qi Specification, Communications Protocol*, list the meanings of the modifiers.

For example, EPT/cc refers to an End Power Transfer data packet having its End Power Transfer code field set to 0x01.

1.6 Power Profiles

A Power Profile determines the level of compatibility between a Power Transmitter and a Power Receiver. Table 3 defines the available Power Profiles.

- *BPP PTx*: A Baseline Power Profile Power Transmitter.
- *EPP5 PTx*: An Extended Power Profile Power Transmitter having a restricted power transfer capability, i.e. $P_L^{(pot)} = 5 \text{ W}$.
- *EPP PTx*: An Extended Power Profile Power Transmitter.
- *BPP PRx*: A Baseline Power Profile Power Receiver.
- *EPP PRx*: An Extended Power Profile Power Receiver.

Table 3: Capabilities included in a Power Profile

Feature	BPP PTx	EPP5 PTx	EPP PTx	BPP PRx	EPP PRx
Ax or Bx design	Yes	Yes	No	N/A	N/A
MP-Ax or MP-Bx design	No	No	Yes	N/A	N/A
Baseline Protocol	Yes	Yes	Yes	Yes	Yes
Extended Protocol	No	Yes	Yes	No	Yes
Authentication	N/A	Optional	Yes	N/A	Optional

2 Introduction

Figure 2 provides a simplified model of a wireless power system, consisting of six blocks. The three blocks to the left of the power transfer interface represent a Power Transmitter and its supply. The three to the right represent a Power Receiver and its Load. Typically, these blocks comprise the following elements.

Supply: in many cases a separate adapter such as a USB PD brick.

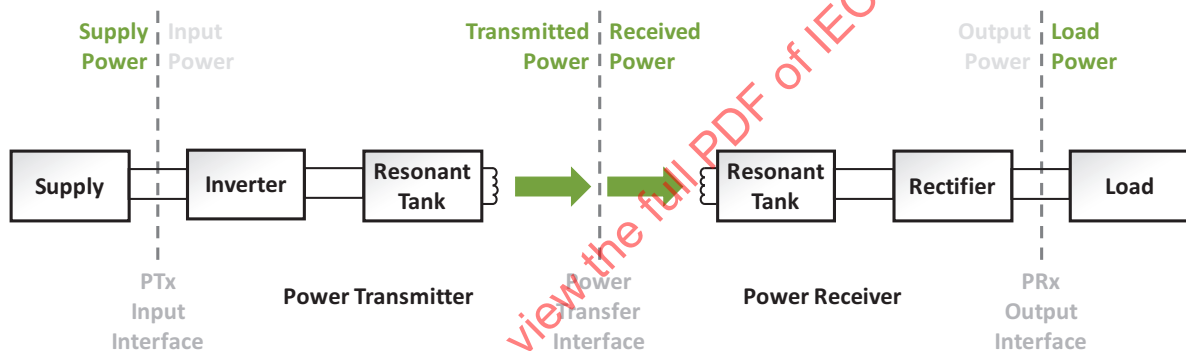
Inverter: a half-bridge or full-bridge for DC/AC conversion.

Resonant Tank: a coil and series capacitor boosting the power transfer capability.

Rectifier: either a diode bridge or an active (synchronous) bridge for AC/DC conversion.

Load: a power sink drawn by the Power Receiver Product, typically a mobile phone's power input to an internal battery charger.

Figure 2. Simplified model of a wireless power transfer system



With reference to Figure 2, the following definitions are central to the understanding of a wireless power system.

Power Signal—An alternating magnetic field.

Supply Power—The power dissipated from the supply.

Power Transmitter—A subsystem that can generate a Power Signal.

Power Transmitter Product—A device containing one or more Power Transmitters.

Transmitted Power—The power from the Power Signal dissipated by any object that is not an integral part of the Power Transmitter Product.

Power Receiver—A subsystem that can extract electric power from a Power Signal.

Power Receiver Product—A device containing a Power Receiver.

Received Power—The power from the Power Signal dissipated by any component that is an integral part of the Power Receiver Product.

Test Power Transmitter—A Power Transmitter Product designed to analyze and check the operation of a Power Receiver Product's wireless power functionality.

Test Power Receiver—A Power Receiver Product designed to analyze and check the operation of a Power Transmitter Product's wireless power functionality.

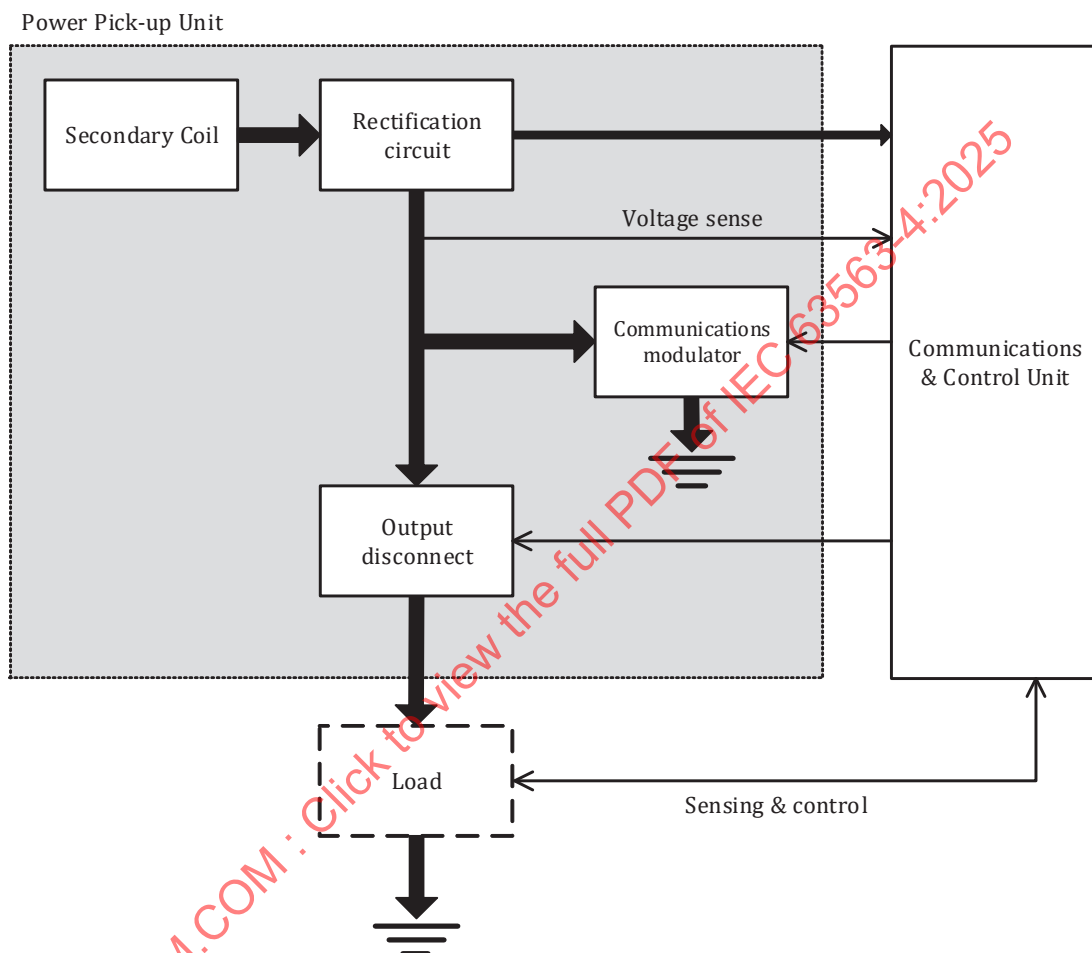
Load Power—The power dissipated in the Load.

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3 Power Receiver construction

Figure 3 illustrates an example of a functional block diagram for a Baseline Power Profile Power Receiver.

Figure 3. Functional block diagram for a Baseline Power Profile Power Receiver



In this example, the Power Receiver consists of a Power Pick-up Unit and a Communications and Control Unit. The Power Pick-up Unit on the left-hand side of Figure 3 comprises the analog components of the Power Receiver:

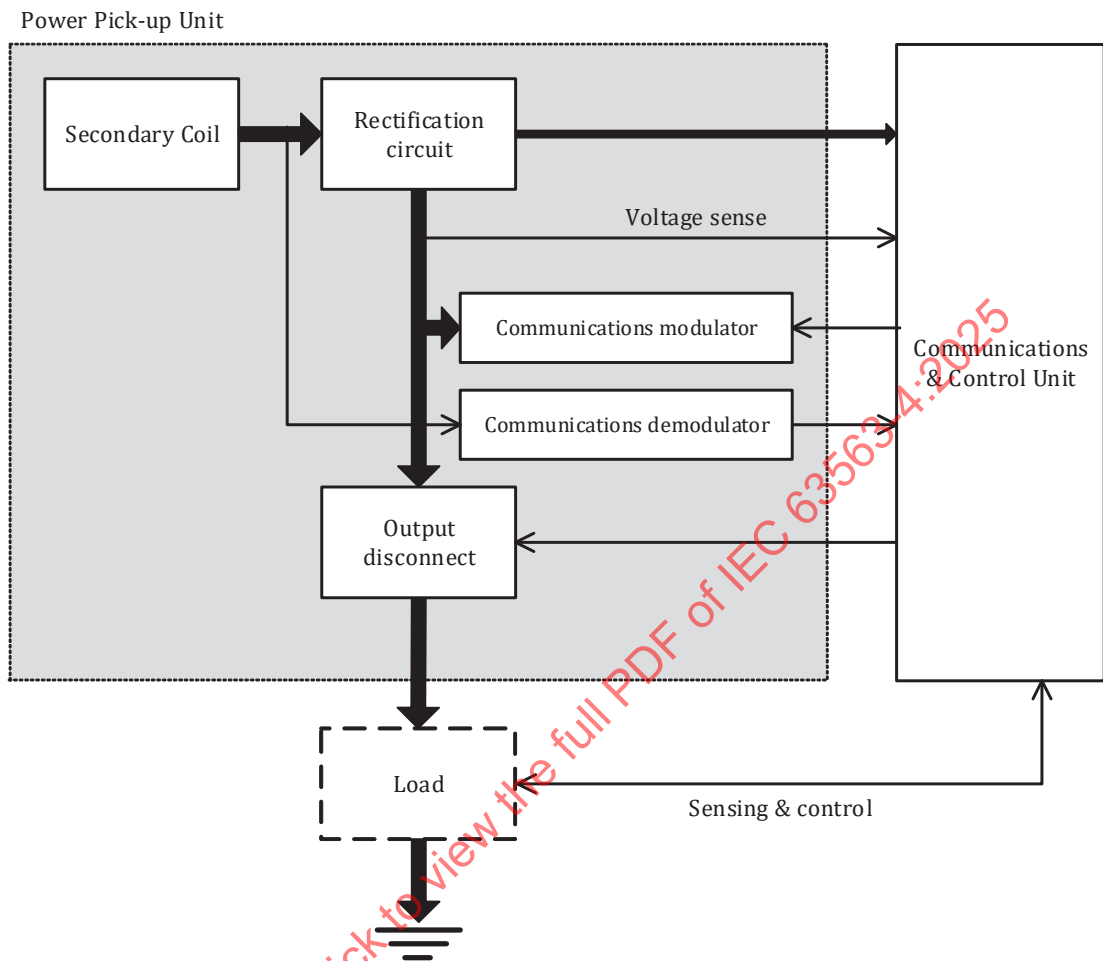
- A dual resonant circuit consisting of a Secondary Coil plus series and parallel capacitances to enhance the power transfer efficiency and enable a resonant detection method (see Section 3.1, *Dual resonant circuit*).
- A rectification circuit that provides full-wave rectification of the AC waveform using, for example, four diodes in a full-bridge configuration or a suitable configuration of active components (see Section 3.2, *Rectification circuit*). The rectification circuit may perform output smoothing as well. In this example, the rectification circuit provides power to both the Communications and Control Unit of the Power Receiver and the output of the Power Receiver.

- A communications modulator (see [Section 3.4, Communications modulator](#)). On the DC side of the Power Receiver, the communications modulator typically consists of a resistor in series with a switch. On the AC side of the Power Receiver, the communications modulator typically consists of a capacitor in series with a switch (not shown in [Figure 3](#)).
- An output disconnect switch, which prevents current from flowing to the output when the Power Receiver does not provide power at its output. In addition, the output disconnect switch prevents current back flow into the Power Receiver when the Power Receiver does not provide power at its output. Moreover, the output disconnect switch minimizes the power that the Power Receiver draws from the Power Transmitter when a Power Signal is first applied to the Secondary Coil.
- A rectified voltage sense.

The Communications and Control Unit on the right-hand side of [Figure 3](#) comprises the digital logic part of the Power Receiver. This unit executes the relevant power control algorithms and protocols, drives the communications modulator, controls the output disconnect switch, and monitors several sensing circuits in both the Power Pick-up Unit and the load. (A good example of a sensing circuit in the load is a circuit that measures the temperature of a rechargeable battery.)

NOTE: This version of the Specification minimizes the set of Power Receiver design requirements defined in this section. Accordingly, compliant Power Receiver designs that differ from the sample functional block diagram shown in [Figure 3](#) are possible. For example, an alternative design includes post-regulation of the output of the rectification circuit (e.g., by using a buck converter, battery charging circuit, power management unit, etc.). In yet another design, the Communications and Control Unit interfaces with other subsystems of the Power Receiver Product, e.g. for user interface purposes.

[Figure 4](#) illustrates an example of a functional block diagram for an Extended Power Profile Power Receiver. The communications demodulator enables the communication of data from the Power Transmitter to an Extended Power Profile Power Receiver. The presence of a communications demodulator is the only difference with the functional block diagram of a Baseline Power Profile Power Receiver.

Figure 4. Functional block diagram for an Extended Power Profile Power Receiver

Power Pick-up Unit components are described in the subsections below.

A Power Receiver design shall include a dual resonant circuit as defined in [Section 3.1, Dual resonant circuit](#), a rectification circuit as defined in [Section 3.2, Rectification circuit](#), sensing circuits as defined in [Section 3.3, Sensing circuits](#), a communications modulator as defined in [Section 3.4, Communications modulator](#), and an output disconnect switch as defined in [Section 3.6, Output disconnect](#).

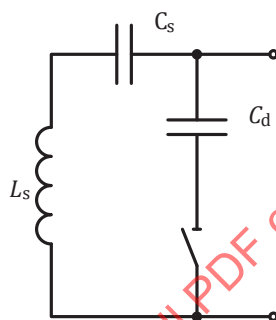
A Power Receiver design for the Extended Power Profile shall also include a communications demodulator as defined in [Section 3.5, Communications demodulator](#), and shall be able to function meaningfully if the Power Transmitter restrictions limit the output of power from the Power Receiver to 5 W; see [Section 3.7, Shielding](#).

3.1 Dual resonant circuit

The dual resonant circuit of the Power Receiver comprises the Secondary Coil and two resonant capacitances. The purpose of the first resonant capacitance C_s is to enhance the power transfer efficiency. The purpose of the second resonant capacitance C_d is to enable a resonant detection of the receiver position on some Power Transmitter designs.

Figure 5 illustrates the dual resonant circuit. The switch in the dual resonant circuit is optional. If the switch is not present, the capacitance C_d shall have a fixed connection to the Secondary Coil L_s . If the switch is present, it shall remain closed¹ until the Power Receiver transmits its first Packet (see the *Qi Specification, Communications Protocol*).

Figure 5. Dual resonant circuit of a Power Receiver



The dual resonant circuit shall have the following resonant frequencies:

$$f'_s = \frac{1}{2\pi \cdot \sqrt{L'_s \cdot C_s}} = 100^{+x}_{-y} \text{ kHz},$$

$$f_d = \frac{1}{2\pi \cdot \sqrt{L_s \cdot \left(\frac{1}{C_s} + \frac{1}{C_d}\right)^{-1}}} = (1000 \pm 10\%) \text{ kHz}.$$

In these equations, L'_s is the self-inductance of the Secondary Coil when placed on the Interface Surface of a Power Transmitter and—if necessary—aligned to the Primary Cell; and L_s is the self-inductance of the Secondary Coil without magnetically active material that is not part of the Power Receiver design close to the Secondary Coil (e.g. away from the Interface Surface of a Power Transmitter). Moreover, the tolerances x and y on the resonant frequency f'_s are $x = y = 5\%$ for Power Receivers that specify a Maximum Power value in the Configuration Packet of 3 W and above, and $x = 5\%$ and $y = 10\%$ for all other Power Receivers.

NOTE: When determining the capacitance value C_d , make sure to account for any parasitic capacitances between the terminals of the dual resonant circuit that may affect the resonance frequency value f_d .

¹ The switch shall remain closed even if no power is available from the Secondary Coil.

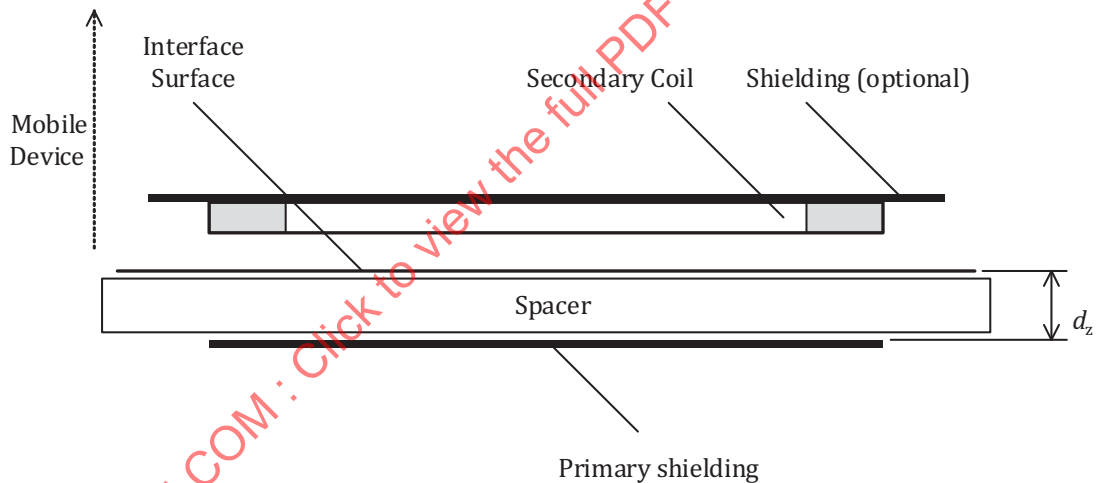
The quality factor Q of the loop consisting of the Secondary Coil, switch (if present), resonant capacitance C_s and resonant capacitance C_d , shall exceed the value 77. Here the quality factor Q is defined as:

$$Q = \frac{2\pi \cdot f_d \cdot L_s}{R}$$

where R is the DC resistance of the loop with the capacitances C_s and C_d short-circuited.

Figure 6 shows the environment that is used to determine the self-inductance L'_s of the Secondary Coil. The primary Shielding shown in Figure 6 consists of material PC44 from TDK Corp. The primary Shielding has a square shape with a side of 50 mm and a thickness of 1 mm. The center of the Secondary Coil and the center of the primary Shielding shall be aligned. The distance from the Receiver Interface Surface to the primary Shielding is $d_z = 3.4$ mm. Shielding on top of the Secondary Coil is present only if the Receiver design includes such Shielding. Other Power Receiver Product components that influence the inductance of the Secondary Coil shall be present as well when determining the resonant frequencies. The excitation signal that is used to determine L_s and L'_s shall have an amplitude of 1 V RMS and a frequency of 100 kHz.

Figure 6. Characterization of resonant frequencies



3.2 Rectification circuit

The rectification circuit shall use full-wave rectification to convert the AC waveform to a DC power level.

3.3 Sensing circuits

The Power Receiver shall monitor the DC voltage V_r directly at the output of the rectification circuit.

3.4 Communications modulator

The Power Receiver shall have the means to modulate the Primary Cell current and Primary Cell voltage as defined in *Qi Specification, Communications Physical Layer*.² This version of the Specification leaves the specific loading method as a design choice to the Power Receiver. Typical methods include modulation of a resistive load on the DC side of the Power Receiver and modulation of a capacitive load on the AC side of the Power Receiver.

3.5 Communications demodulator

For the Extended Power Profile, the Power Receiver shall have the means to demodulate frequency-shift keying (FSK) data from the Power Signal frequency as defined in *Qi Specification, Communications Physical Layer*. This Specification leaves the specific method up to the designer of the Power Receiver.

3.6 Output disconnect

The Power Receiver shall have the means to disconnect its output from the subsystems connected thereto. If the Power Receiver has disconnected its output, it shall ensure that it still draws a sufficient amount of power from the Power Transmitter, such that Power Receiver to Power Transmitter communications remain possible (see *Qi Specification, Communications Physical Layer*).

The Power Receiver shall keep its output disconnected until it reaches the *power transfer* phase for the first time after a Digital Ping (see the *Qi Specification, Communications Protocol*). Subsequently, the Power Receiver may operate the output disconnect switch any time while the Power Transmitter applies a Power Signal.

NOTE: The Power Receiver may experience a voltage peak when operating the output disconnect switch (and changing between maximum and near-zero power dissipation).

² Note that the dual resonant circuit as depicted in [Figure 5 \(in Section 3.1\)](#) does not prohibit implementation of the communications modulator directly at the Secondary Coil.

3.7 Shielding

An important consideration for a Power Receiver designer is the impact of the Power Transmitter's magnetic field on the Power Receiver Product. Stray magnetic fields could interact with the Power Receiver Product and potentially cause its intended functionality to deteriorate or cause its temperature to increase due to the power dissipation of generated eddy currents.

It is recommended to limit the impact of magnetic fields by means of Shielding on the top face of the Secondary Coil (see the *Qi Specification, Mechanical, Thermal, and User Interface* for a diagram of the secondary coil assembly). This Shielding should consist of material that has parameters similar to the materials listed in the *Qi Specification*. The Shielding should cover the Secondary Coil completely. Additional Shielding beyond the outer diameter of the Secondary Coil might be necessary depending upon the impact of stray magnetic fields.

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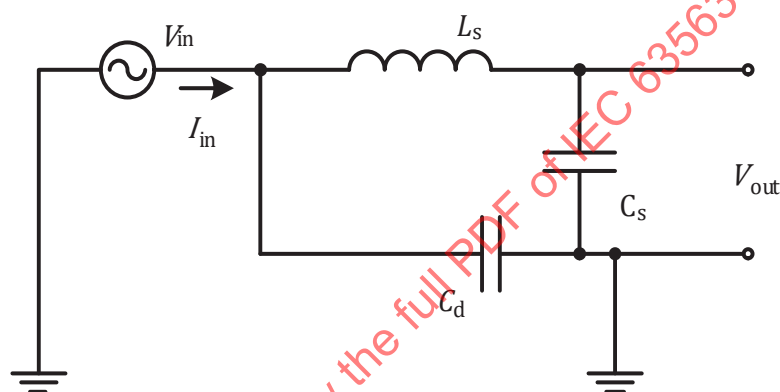
4 Power Receiver design guidelines (informative)

4.1 Large-signal resonance check

In the course of designing a Power Receiver, it should be verified that the resonance frequency f_s of the dual resonant circuit remains within the tolerance range defined in [Section 3.1, Dual resonant circuit](#), under large-signal conditions. The test defined in this section serves this purpose.

Step 1. Connect an RF power source to the assembly of Secondary Coil, Shielding and other components that influence the inductance of the Secondary Coil and series resonant capacitance C_s ; see [Figure 7](#). The presence of the parallel capacitance C_d is optional.

Figure 7. Large signal secondary resonance test



Step 2. Position the assembly and an appropriate spacer on primary Shielding material, as shown in [Figure 5 \(in Section 3.1\)](#).

Step 3. Measure the input voltage V_{in} as a function of the frequency of the RF power source in the range of 90...110 kHz, while maintaining the input current I_{in} at a constant level, preferably at about twice the maximum value intended in the final product.

Step 4. Verify that the frequency at which the measured V_{in} is at a minimum, occurs within the specified tolerance range of the resonance frequency f_s .

4.2 Power Receiver coil design

The mutual inductance M of a Secondary Coil, in combination with optional Shielding and other Power Receiver Product components, and the Primary Coil of a Power Transmitter design A10 should satisfy the following relations:

- $\frac{V_o}{\omega M} < 0.8 \text{ A}$, if the Primary Coil and Secondary Coil centers are aligned; and
- $\frac{V_o}{\omega M} < 1 \text{ A}$, if the Primary Coil and Secondary Coil centers have a lateral offset of $5\sqrt{2} \text{ mm}$.

Here V_o is the maximum output voltage expected from the Secondary Coil—or any other voltage that the Power Receiver designer considers relevant—and $\omega = 2\pi f$, with $f = 100 \text{ kHz}$, the frequency at which the mutual inductance (in units of 1 henry) is measured.

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5 Power Transmitter construction

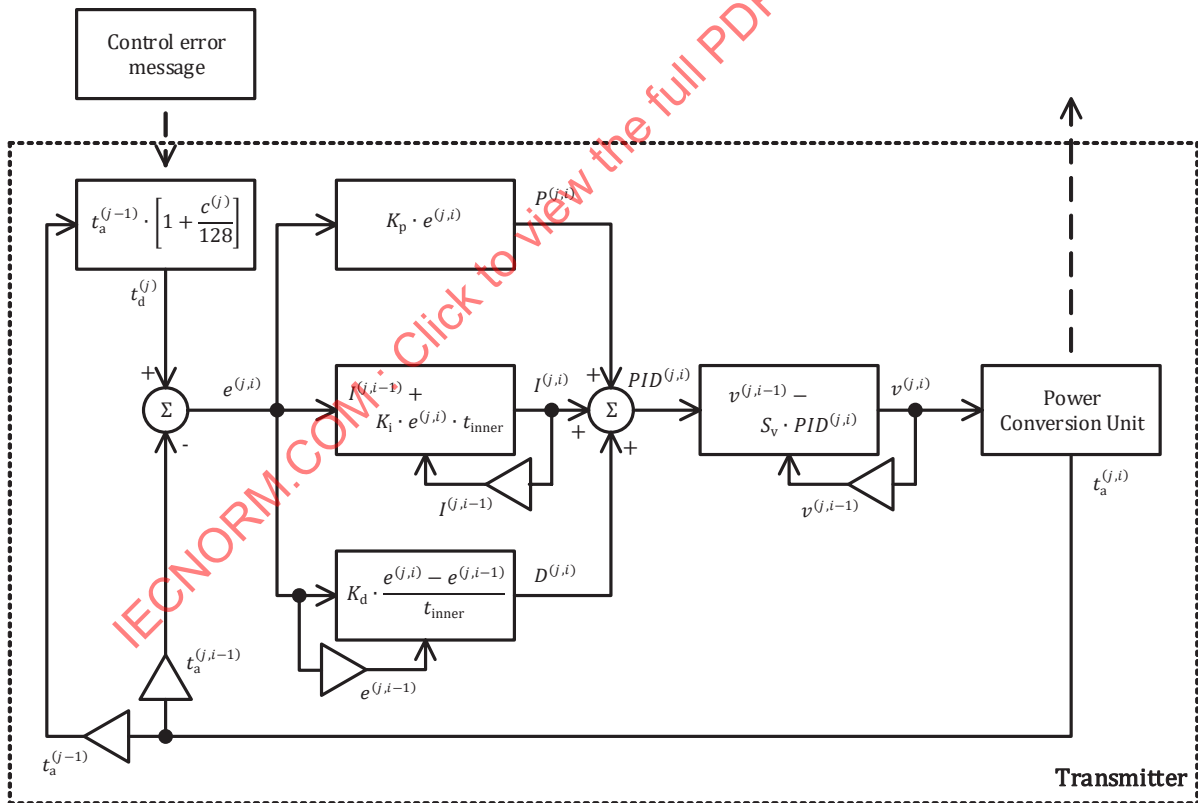
5.1 Power Transmitter reference designs

The *Qi Specification* includes a set of Power Transmitter reference designs that were developed, tested, and certified by member companies of the Wireless Power Consortium.

5.2 Power transfer control

This version of the Specification, defines a specific method, which the Power Transmitter shall use to control its Primary Cell current towards the new Primary Cell current [see *Qi Specification, Communications Protocol* for a description of the power transfer phases). This method is based on a discrete proportional-integral-differential (PID) algorithm as illustrated in Figure 8.

Figure 8. PID control algorithm



To execute this algorithm, the Power Transmitter shall execute the steps listed below, in the order of appearance. In the definitions of these steps, the index $j = 1, 2, 3, \dots$ labels the sequence of Control Error Packets, which the Power Transmitter receives.

- Upon receipt of the j^{th} Control Error Packet, the Power Transmitter shall calculate the new Primary Cell current $t_d^{(j)}$ as

$$t_d^{(j)} = t_a^{(j-1)} \cdot \left[1 + \frac{c^{(j)}}{128} \right]$$

where $t_a^{(j-1)}$ represents the actual Primary Cell current—reached in response to the previous Control Error Packet—and $c^{(j)}$ represents the Control Error Value contained in the j^{th} Control Error Packet. Note that $t_a^{(0)}$ represents the Primary Cell current at the start of the power transfer phase.

- If the Control Error Value $c^{(j)}$ is non-zero, the Power Transmitter shall adjust its Primary Cell current during a time window t_{active} . For this purpose, the Power Transmitter shall execute a loop comprising of the steps listed below. The index $i = 1, 2, 3, \dots, i_{\text{max}}$ labels the iterations of this loop.
 - The Power Transmitter shall calculate the difference between the new Primary Cell and the actual Primary Cell current as the error

$$e^{(j,i)} = t_d^{(j)} - t_a^{(j,i-1)}$$

where $t_a^{(j,i-1)}$ represents the Primary Cell current determined in iteration $i - 1$ of the loop. Note that $t_a^{(j,0)}$ represents the actual Primary Cell current at the start of the loop.

- The Transmitter shall calculate the proportional, integral, and derivative terms (in any order):

$$P^{(j,i)} = K_p \cdot e^{(j,i)}$$

$$I^{(j,i)} = I^{(j,i-1)} + K_i \cdot e^{(j,i)} \cdot t_{\text{inner}}$$

$$D^{(j,i)} = K_d \cdot \frac{e^{(j,i)} - e^{(j,i-1)}}{t_{\text{inner}}}$$

where K_p is the proportional gain, K_i is the integral gain, K_d is the derivative gain, and t_{inner} is the time required to execute a single iteration of the loop. In addition, the integral term $I^{(j,0)} = 0$, and the error $e^{(j,0)} = 0$. The Power Transmitter shall limit the integral term $I^{(j,i)}$ such that it remains within the range $-M_I \dots + M_I$ —if necessary, the Power Transmitter shall replace the calculated integral term $I^{(j,i)}$ with the appropriate boundary value.

- The Power Transmitter shall calculate the sum of the proportional, integral, and derivative terms:

$$PID^{(j,i)} = P^{(j,i)} + I^{(j,i)} + D^{(j,i)}.$$

In this calculation, the Power Transmitter shall limit the sum $PID^{(j,i)}$ such that it remains within the range $-M_{PID} \dots +M_{PID}$.

- The Power Transmitter shall calculate the new value of the controlled variable

$$v^{(j,i)} = v^{(j,i-1)} - S_v \cdot PID^{(j,i)},$$

where S_v is a scaling factor that depends on the controlled variable. In addition, the controlled variable $v^{(j,0)} = v^{(j-1,i_{\max})}$, with $v^{(0,0)}$ representing the actual value of the controlled variable at the start of the *power transfer* phase, is either the Operating Frequency, the duty cycle of the inverter, or the voltage input to the inverter. If the calculated $v^{(j,i)}$ exceeds the specified range, the Power Transmitter shall replace the calculated $v^{(j,i)}$ with the appropriate limiting value.

The Power Transmitter shall apply the new value of the controlled variable $v^{(j,i)}$ to its Power Conversion Unit.

▫

- The Power Transmitter shall determine the actual Primary Cell current $t_a^{(j,i)}$.

The maximum number of iterations of the loop i_{\max} and the time t_{inner} required to execute a single iteration of the loop shall satisfy the following relation:

$$i_{\max} \cdot t_{\text{inner}} = t_{\text{active}}, \text{ with } 1 \text{ ms} \leq t_{\text{inner}} \leq 5 \text{ ms}$$

- The Power Transmitter shall determine the Primary Cell current $t_a^{(j)}$ exactly at $t_{\text{delay}} + t_{\text{active}} + t_{\text{settle}}$ after the end of the j^{th} Control Error Packet.

See the definition of the individual Power Transmitter designs for the values of K_p , K_i , K_d , M_p , and M_{PID} .

6 Power consumption

In consideration of compliance testing, a Power Receiver shall not drive the Transmitted Power of Test Power Transmitter #2 above 7500 mW with the Power Receiver being positioned on TPT#2 such that power transfer can be sustained without interruption.

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7 Meaningful functionality

(Extended Power Profile) If the Power Receiver is not able to negotiate its intended Guaranteed Load Power level with the Power Transmitter, it shall negotiate a lower Guaranteed Load Power level, and function meaningfully at that power level. Meaningful functionality includes charging a connected battery at a rate lower than intended.

NOTE: The following examples list cases in which the Power Receiver may not be able to negotiate its target operating power.

- The Power Receiver is positioned on a BPP Power Transmitter.
- The Potential Power provided in the Power Transmitter Capability Packet is lower than the Power Receiver's target operating power.
- The Power Transmitter is powered by an external power supply that is designed to provide no more than 5 W of power.

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8 Unintentional Magnetic Field Susceptibility (Informative)

8.1 Limits

It should also be noted that a Power Receiver can be exposed to higher than expected fields during otherwise normal operation. For example, if the Power Receiver is suddenly moved such that its coupling with the Power Transmitter changes significantly, the communications channel can become unusable and the voltage generated across the Secondary Coil can increase unexpectedly.

8.2 Protection

In the case that the output disconnect switch is open, it is recommended that a Power Receiver can withstand a voltage generated across its Secondary Coil of at least U_{ovp} . Here, U_{ovp} is the larger of

- 1.6 times the maximum target rectified voltage as defined in Table 4, or
- the voltage that results if coupled with a type MP-A1 Power Transmitter that is operating at its minimum Operating Frequency and maximum phase difference between the legs of its full-bridge inverter.

Table 4: Examples of the recommended U_{ovp}

Maximum Target Rectified Voltage [V]	Recommended U_{ovp} [V]
12	20
20	32
30	48

8.3 Power Transmitter detection

To detect whether the Power Signal originates from a Power Transmitter, as described in the *Qi Specification, Communications Physical Layer*, the Power Receiver should also take into account the Power Transmitter designs.

9 Load Steps

A Power Receiver Product may perform load steps and dumps that are beyond the control of its Power Receiver. A load step or dump causes an immediate impedance change, which is reflected from the Secondary Coil to the Primary Coil and results in a change of the rectified voltage. Due to the latency of the control loop (which is mainly due to the time that is required to communicate Control Error Packets), it takes a while before the rectified voltage is readjusted to a (new) desired value. The Power Transmitter should ensure that the established Power Transfer Contract is not terminated during such an event. Therefore, an implementation of a Power Transmitter should meet load steps from 10% to 100% of the Maximum Power (as communicated by the Power Receiver in the Configuration Packet) and load dumps from 100% to 10%.

9.1 Load step test procedure

9.1.1 Baseline Power Profile load step test

The following procedure is recommended to verify that the Power Transmitter is able to handle load steps and dumps:

1. Position Test Power Receiver #1 in configuration B on the Interface Surface of the Power Transmitter Product with an initial load of $32\ \Omega$, a Power Control Hold-off Time of $t_{\text{delay}} = 100\ \text{ms}$, and an interval time between consecutive Control Error Packets of $t_{\text{interval}} = 250\ \text{ms}$.
2. Establish communication and regulate the rectified voltage to $V_r = (7 \pm 2\%)\ \text{V}$.
3. Change the load from its initial value to $127\ \Omega$ and regulate the rectified voltage to $V_r = (7 \pm 2\%)\ \text{V}$.
4. Change the load from $127\ \Omega$ to $10\ \Omega$, $\Delta t_1 = 50\ \text{ms}$ before sending a Control Error Packet.
5. Verify that the Test Power Receiver continues to regulate and that the Power Transmitter Product responds to the Control Error Packets by adjusting V_r .
6. Measure the rectified voltage (V_0 , V_1 , and V_{min}) with timings as shown in Figure 9, where $\Delta t_2 = 1800\ \text{ms}$.
7. Verify that the measured values comply with the limits provided in Table 5.

Figure 9. Load step test diagram

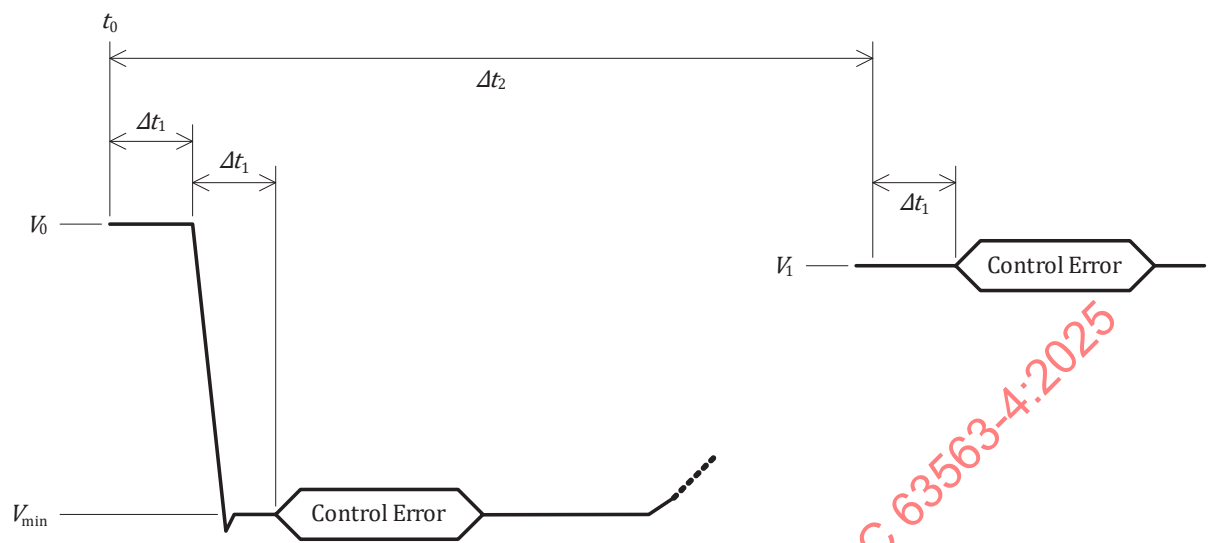


Table 5: Load step limits

Voltage	Minimum	Target	Maximum	Unit
V_0	6.9	7	7.1	V
V_{min}	4	7	7.1	V
V_1	6	V_0	7.1	V

9.1.2 Extended Power Profile load step test

1. Position the Test Power Receiver on the Interface Surface of the Power Transmitter Product, with an initial load of R_{init} , a Power Control Hold-off Time of $t_{\text{delay}} = 100$ ms, and an interval time between consecutive Control Error Packets of $t_{\text{interval}} = 250$ ms. See Table 6 for relevant parameters.
2. Establish communications and regulate the rectified voltage to V_r .
3. Change the load from its initial value to R_{light} and regulate the rectified voltage V_r .
4. Change the load from R_{light} to R_{heavy} at $\Delta t_1 = 50$ ms before a sending a Control Error Packet.
5. Verify that the Test Power Receiver continues to regulate and that the Power Transmitter Product responds to the Control Error Packets by adjusting V_r .
6. Measure the rectified voltages (V_0 , V_1 , and V_{min}) with timings as shown in Figure 9 above, where $\Delta t_2 = 1800$ ms.
7. Verify the measured values with the limits provided in Table 5.

Table 6: Load step definitions

Test Power Receiver	Initial Load R_{init}	Light Load R_{light}	Heavy Load R_{heavy}	Rectified Voltage V_r
TPR#1B	32 Ω	127 Ω	10 Ω	(7 \pm 2%) V
TPR#MP1B	72 Ω	96 Ω	10 Ω	(12 \pm 2%) V

Table 7: Load step limits

Test Power Receiver	Voltage	Minimum [V]	Target [V]	Maximum [V]
TPR#1B	V_0	6.9	7	7.1
	V_{min}	4	7	7.1
	V_1	6	V_0	7.1
TPR#MP1B	V_0	11.8	12	12.2
	V_{min}	6.9	12	12.2
	V_1	10.3	V_0	12.2

9.2 Load dump test procedure

9.2.1 Baseline Power Profile load dump test

1. Position Test Power Receiver #1 in configuration B on the Interface Surface of the Power Transmitter Product, with an initial load of $32\ \Omega$, a Power Control Hold-off Time $t_{\text{delay}} = 100\ \text{ms}$, and an interval time between consecutive Control Error Packets $t_{\text{interval}} = 250\ \text{ms}$.
2. Establish communication and regulate the rectified voltage to $V_r = (7 \pm 2\%) V$.
3. Change the load from its initial value to $10\ \Omega$ and regulate the rectified voltage to $V_r = (7 \pm 2\%) V$.
4. Change the load from $10\ \Omega$ to $127\ \Omega$, $\Delta t_1 = 50\ \text{ms}$ before a sending a Control Error Packet.
5. Verify that the Test Power Receiver continues to regulate and that the Power Transmitter Product responds to the Control Error Packets by adjusting V_r .
6. Measure the rectified voltage (V_0 , V_1 , and V_{min}) with timings as shown in Figure 10, where $\Delta t_2 = 1800\ \text{ms}$.
7. Verify that the measured values comply with the limits provided in Table 8.

Figure 10. Load dump test diagram

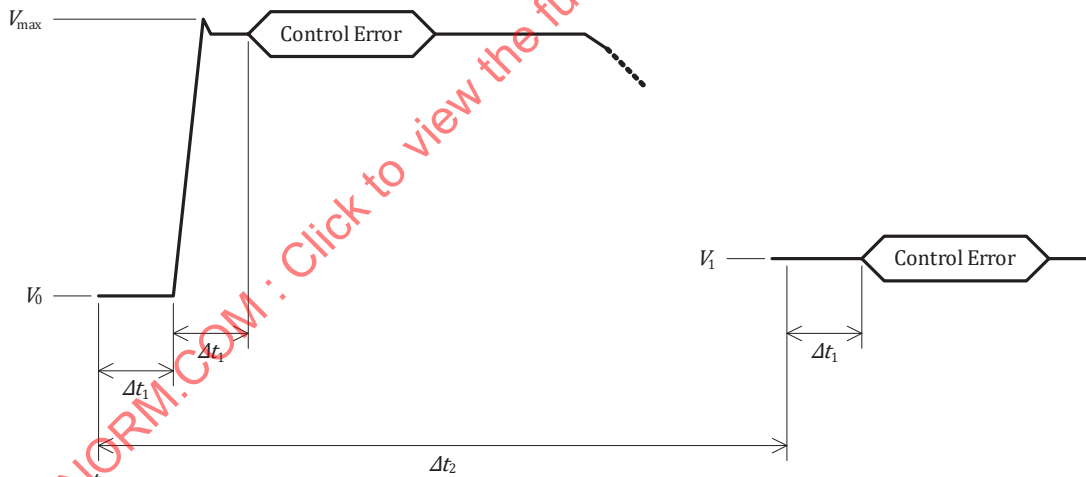


Table 8: Load dump limits (Baseline Power Profile)

Voltage	Minimum	Target	Maximum	Unit
V_0	6.9	7	7.1	V
V_{min}	6.9	7	12	V
V_1	6.9	V_0	8	V

9.2.2 Extended Power Profile load dump test

- Position the Test Power Receiver on the Interface Surface of the Power Transmitter Product, with an initial load of R_{init} , a Power Control Hold-off Time of $t_{delay} = 100$ ms, and an interval time between consecutive Control Error Packets of $t_{interval} = 250$ ms. See Table 9 for the relevant parameters.
- Establish communications and regulate the rectified voltage to V_r .
- Change the load from its initial value to R_{heavy} and regulate the rectified voltage V_r .
- Change the load from R_{heavy} to R_{light} at $\Delta t_1 = 50$ ms before a sending a Control Error Packet.
- Verify that the Test Power Receiver continues to regulate and that the Power Transmitter Product responds to the Control Error Packets by adjusting V_r .
- Measure the rectified voltages (V_0 , V_1 , and V_{min}) with timings as shown in Figure 10 above, where $\Delta t_2 = 1800$ ms.
- Verify the measured values with the limits provided in Table 9.

Table 9: Load dump definitions (Extended Power Profile)

Test Power Receiver	Initial Load R_{init}	Light Load R_{light}	Heavy Load R_{heavy}	Rectified Voltage V_r
TPR#1B	32 Ω	127 Ω	10 Ω	(7 \pm 2%) V
TPR#MP1B	72 Ω	96 Ω	10 Ω	(12 \pm 2%) V

Table 10: Load dump limits

Test Power Receiver	Voltage	Minimum [V]	Target [V]	Maximum [V]
TPR#1B	V_0	6.9	7	7.1
	V_{min}	6.9	7	12
	V_1	6.9	V_0	8
TPR#MP1B	V_0	11.8	12	12.2
	V_{min}	11.8	12	20.5
	V_1	11.8	V_0	13.7

10 Over-voltage protection

A Power Transmitter shall limit the amplitude of its Power Signal (or magnetic field strength) such that it does not generate a rectified voltage higher than 20 V at the output of a properly designed Power Receiver.

The Power Signal depends on the amount of current that runs through the Primary Coil. This amount is primarily determined by the Power Transmitter's Operating Point, the Power Receiver's load impedance, and the coupling between the Primary Coil and Secondary Coil. Whereas the Power Receiver can—to a certain extent—control its load impedance and the Power Transmitter's Operating Point by transmitting appropriate Control Error Packets, it has little control over the coupling. As a consequence, scenarios exist in which a higher-than-expected voltage can result at the Power Receiver's output.

In one scenario, the user initially places the Power Receiver at a position where the coupling is poor and subsequently moves it to a position where the coupling is strong. In practice this can happen when the user keeps the Power Receiver hovering at a small distance above the Interface Surface before setting it down, or when the user places the Power Receiver with a large misalignment between the Primary Coil and Secondary Coil and subsequently slides it into better alignment.

In either case, the Power Transmitter can detect the Power Receiver and establish communications before the coils are properly aligned. The Power Receiver can then start to control its output voltage to a higher level, such as 12 V, in order to prepare for connecting its load. If the coupling is poor, the Power Receiver typically can reach its target voltage only by driving the power Transmitter to use a high Primary Coil current (and therefore a strong Power Signal or high magnetic field). If the coupling suddenly improves substantially, as in the above scenarios, the Power Receiver does not have time to drive the Power Transmitter back to a lower Primary Coil current. As a result, its output voltage can substantially increase—up to tens of volts if no special precautions are taken.

Many Power Receiver implementations that are based on common IC technology cannot handle such voltages, with 20 V being a safe upper limit. Moreover, design constraints often are of such a nature that commonly used solutions for over-voltage protection cannot be applied. For example, large Zener diodes or dummy loads that can handle the excess power typically are too bulky to fit in space-limited designs. Accordingly, the Power Receiver typically has no alternative but to rely on the Power Transmitter to keep its voltage below the safe limit.

Whereas a Power Transmitter can hold its Primary Coil current to a sufficiently low level, placing a hard limit on the Primary Coil current can prevent a Power Receiver from reaching its target power level when it has connected its load.

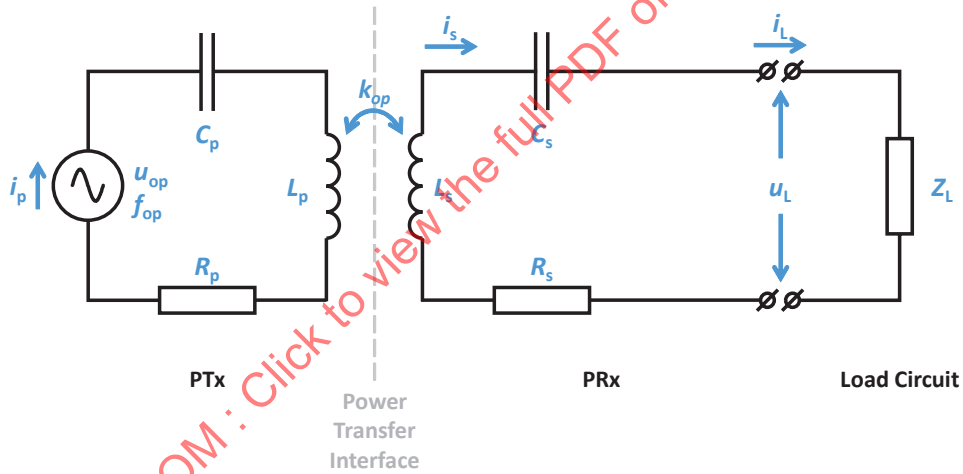
A better solution is to define more than one limit according to the amount of power that is transmitted:

- The Power Transmitter should use a low current limit if the Transmitted Power is low to prevent an over-voltage from occurring in the Power Receiver
- It should use a high current limit if the Transmitted Power is high to enable the Power Receiver to reach its target Operating Point without creating an over-voltage in the Power Receiver.

The system model and analysis below explain this approach in more detail.

Figure 11 illustrates a simplified model of the system comprising a Power Transmitter on the left and a Power Receiver on the right. For clarity, the load circuit is drawn separately from the Power Receiver. The Power Transmitter consists of a power source (u_{op}, f_{op}), a capacitance C_p , an inductance L_p , and a resistance R_p . The power source supplies a sinusoidal voltage u_{op} at a frequency f_{op} . The Power Receiver consists of a capacitance C_s , an inductance L_s , and a resistance R_s . A load having an impedance Z_L is connected to the output terminals of the Power Receiver. The symbols u_L , i_L , i_p , and k_{op} represent the load voltage, load current, Primary Coil current, and coupling factor.

Figure 11. Simplified system model



For simplicity, the Power Receiver in the model includes neither a rectifier nor a resonance at a frequency f_a as defined in [Section 3.1, Dual resonant circuit](#) and [Section 3.2, Rectification circuit](#). The absence of the additional resonance does not significantly affect the results discussed below. The effect of the rectifier is described at the end of this section.

Table 11 lists the parameters associated with the system model in Figure 11. Instead of the resonant capacitances C_p and C_s , and the resistances R_p and R_s , the resonant frequencies f_p and f_s , and quality factors Q_p and Q_s are provided. The relations between these parameters are as follows:

$$f_p = \frac{1}{2\pi\sqrt{L_p C_p}}, \quad f_s = \frac{1}{2\pi\sqrt{L_s C_s}}, \quad Q_p = \frac{2\pi f_p L_p}{R_p}, \quad Q_s = \frac{2\pi f_s L_s}{R_s}$$

The Power Transmitter controls the amount of power it transfers by adjusting the amplitude of its voltage and frequency in the ranges given in Table 11.

At start-up, it uses the ping voltage u_{ping} and ping frequency f_{ping} . To control the power up, it decreases its frequency while keeping its voltage constant at the maximum value. To control the power down, it increases the frequency at constant voltage, and after reaching the maximum frequency value decreases the voltage while keeping the frequency constant at that maximum.

At start-up, the Power Receiver uses a load impedance Z_{ping} , which represents the load of its control electronics such as a microprocessor. After start-up, the Power Receiver can adjust its load impedance to reach its target Operating Point as given by the target voltage u_L and target current i_L .

Table 11: Parameters of the simplified model

Power Transmitter			Power Receiver		
L_p	25	μH	L_s	35	μH
f_p	100	kHz	f_s	100	kHz
Q_p	100		Q_s	40	
u_{op}	2...24	V (pk)	u_L	12	V (rms)
f_{op}	100...200	kHz	i_L	1.5	A (rms)
u_{ping}	24	V (pk)	Z_L	0.1...1000	Ω
f_{ping}	175	kHz	Z_{ping}	800	Ω

Power Transmitter operation is subject to these constraints:

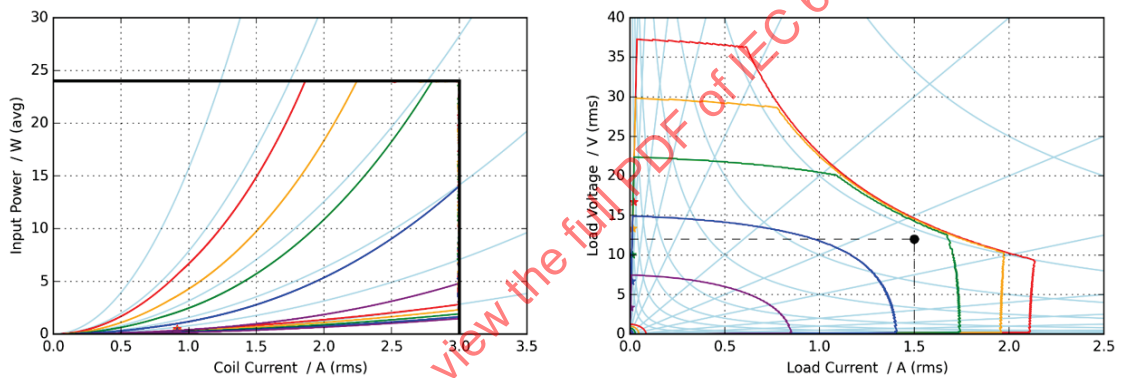
- The Power Transmitter only uses the part of its Operating Frequency range where the Primary Coil current decreases while the Operating Frequency increases. This constraint ensures that the Control Error Packets from the Power Receiver have a consistent effect: a positive Control Error Value causes the Primary Coil current to increase, and a negative Control Error Value causes the Primary Coil current to decrease.

NOTE: A positive Control Error Value directs the Power Transmitter to increase its voltage, or to decrease its Operating Frequency if the voltage has reached its maximum value. A negative Control Error Value directs the Power transmitter to increase its Operating Frequency, or to decrease its voltage if the Operating Frequency has reached its maximum value. This method of power control is used by many Power Transmitter designs.

- The Power Transmitter limits the amount of power that it takes from its power source. In the simplified model, the maximum average power is 24 W.
- The Power Transmitter limits the amount of Primary Coil current. Two examples are discussed below. In the first example, the Primary Coil current is limited at the fixed value of 3 A rms. In the second example, the Primary Coil current limit depends on the Transmitted Power, increasing from 0.75 A (rms) at near zero Transmitted Power up to about 2.7 A (rms) at near maximum Transmitted Power.

The diagram on the left in Figure 12 illustrates the full operating space of the Power Transmitter in terms of its Primary Coil current and the power it takes from its power source. The diagram on the right illustrates the operating space of the Power Receiver in terms of its load current and voltage. The solid black lines in the Power Transmitter's diagram indicate its power and current limits. The solid black dot in the Power Receiver's diagram indicates its target Operating Point. The colors of the different curves represent different coupling factors. The red curve corresponds to a coupling factor of 0.56 (good coupling). The yellow, green, blue, and purple curves correspond to 80%, 60%, 40%, and 20% of the "red" value. Each curve forms a closed contour limiting the operating space of the Power Transmitter and Power Receiver for the associated coupling factor (for the parts of the contour that coincide with the power limit, the current limit, or the diagram axes this may be difficult to see). The Power Transmitter and Power Receiver can reach any point within a contour given appropriate values of the Power Transmitter's Operating Frequency and voltage. Finally, the stars indicate the ping Operating Points of the Power Transmitter and Power Receiver.

Figure 12. Operating space with a fixed-maximum Primary Coil current

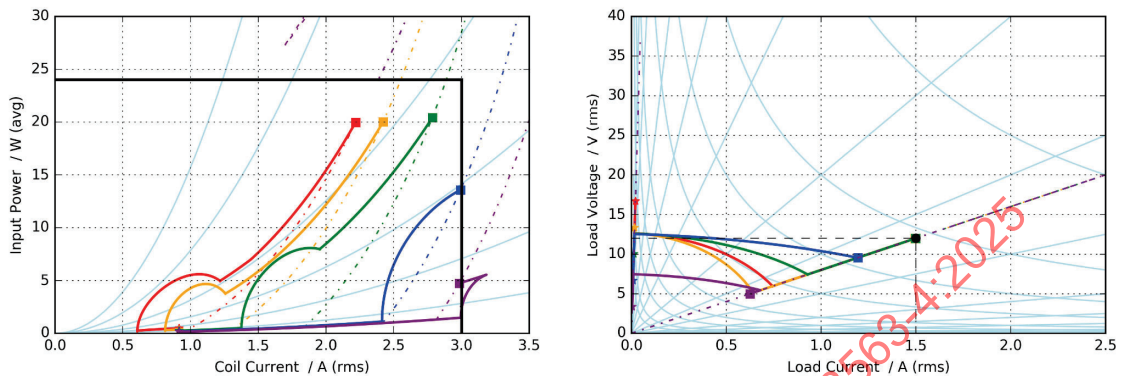


The diagram on the right shows that the Power Receiver can reach its target Operating Point for a coupling factor greater than about 0.3, because that Operating Point lies well within the green contour (a coupling factor of $60\% \cdot 0.56$). The diagram also makes clear that the load voltage can potentially reach levels well above 20 V (rms) for coupling factors greater than 0.3. For example, the top left corner of the yellow curve, representing a coupling factor of $80\% \cdot 0.56$ and a load impedance of 1 k Ω , reaches a load voltage of 30 V (rms).

The solid curves in Figure 13 illustrate the "trajectories" that the Power Transmitter and Power Receiver follow through their operating space when controlling from the ping Operating Point to the target Operating Point at different coupling factors. Each trajectory starts from the ping Operating Point, which is indicated by a star. The Power Receiver first controls its load voltage to a value just over 12 V (rms). In the Transmitter's diagram this is the slightly slanted line near the bottom (less than 1 W of input power). In the Power Receiver it is the steep line close to the vertical axis. Next the Power Receiver changes its load from the ping load impedance to the target load impedance ($12 \text{ V} / 1.5 \text{ A} = 8 \Omega$). This load step increases the Power Transmitter's power and Primary Coil current, and it decreases the load voltage. For the lowest coupling (purple curve) the Primary coil current even exceeds the limit. In this example, the Power Transmitter does not enforce its current limit instantly, but instead controls its Operating Point back to the limit after completion of the load step. Finally, the Power Receiver controls its voltage to the target value, which is possible for the highest coupling factors only (red, yellow, and green curves).

At the lower coupling factors (blue and purple curves), the Power Transmitter hits its current limit. The solid squares indicate the final Operating Point for each coupling factor.

Figure 13. System control with a fixed-maximum Primary Coil current (1)



As a clear illustration of the scenarios described earlier in this section, the dashed and dotted curves in Figure 13 show the trajectories that the Power Transmitter and Power Receiver follow if the coupling factor changes between zero and 0.56. The load impedance and the Power Transmitter's Operating Point are fixed on these trajectories (i.e. the Power Transmitter does not enforce its limits during the coupling step). As shown in the diagram on the right, the load voltage can reach values up to about 20 V (rms) at the target load impedance of 8 Ω .

To reach this voltage, the input power and Primary Coil current exceed their limits substantially (see the left diagram). The behavior is radically different at the ping impedance of 800 Ω , where the load voltage can reach values well over 20 V (rms). Corresponding trajectories are not visible in the diagram on the left because the coupling step causes hardly any change in the Primary Coil current and input power.

Even if the Power Transmitter would instantly enforce its limits, the load voltage would reach these high levels. This is clearly visible in Figure 14, where the maximum load voltage is much reduced at the target load impedance but not at the ping impedance. In fact, the maximum reachable load voltages can be read directly from the red contour in Figure 12 (diagram on the right).

Figure 14. System control with a fixed-maximum Primary Coil current (2)

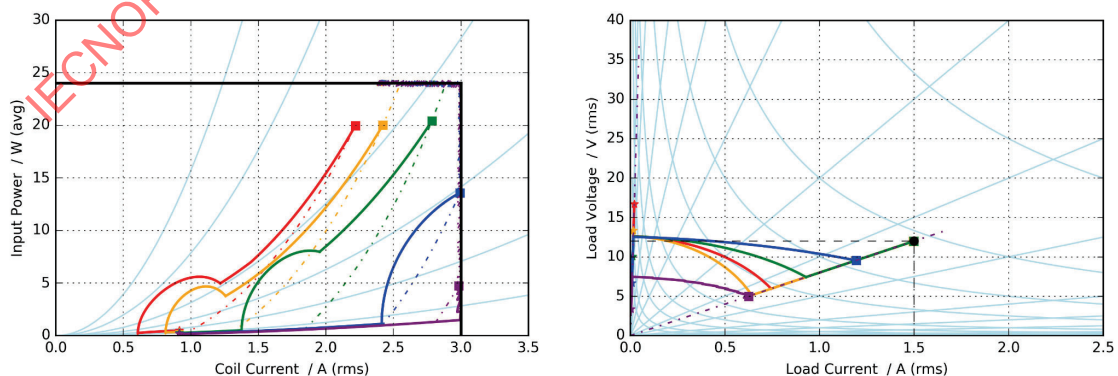
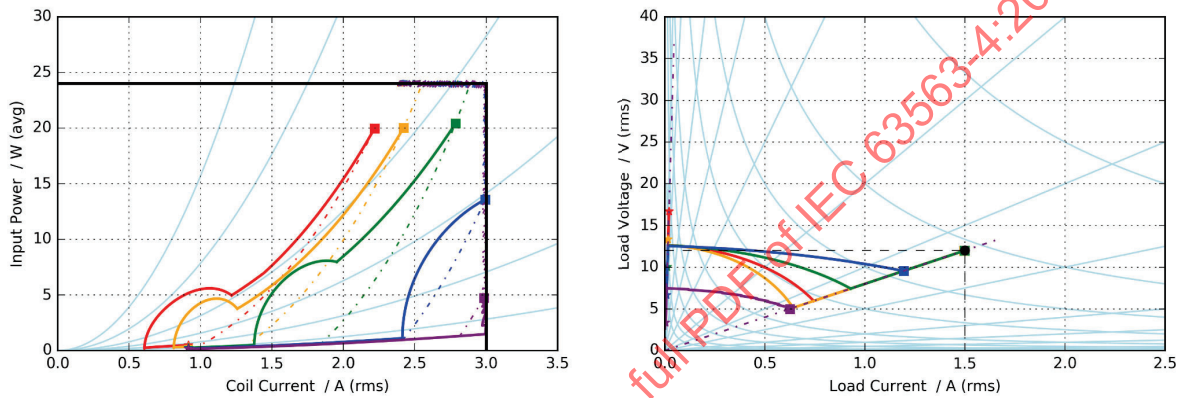


Figure 15 illustrates that a Primary Coil current limit that depends on the Transmitted Power (or on the input power) is a means to mitigate high load voltages in the Power Receiver. Clearly, the highest load voltages reached using this limit stay well below 20 V (rms). This example also illustrates that the cost of this approach is a reduced coupling range over which the Power Receiver can reach its target Operating Point (the green curve representing a coupling factor of $60\% \cdot 0.56$ no longer reaches the target Operating Point).

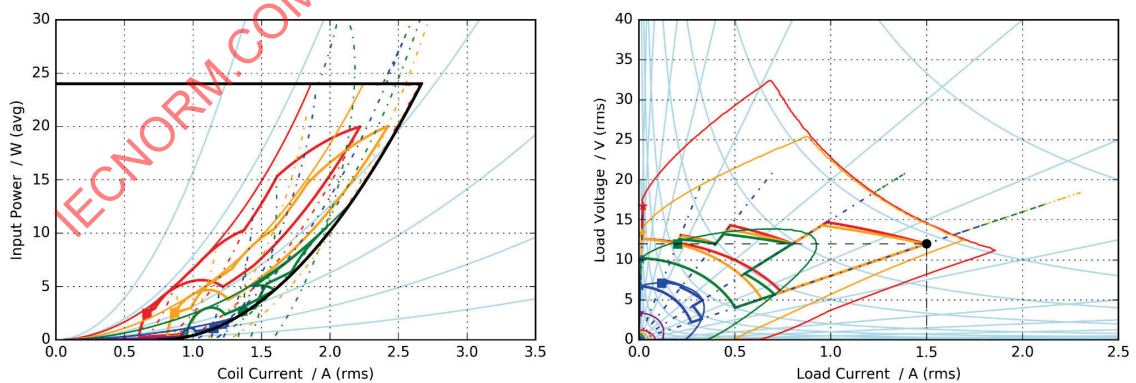
This means that proper alignment of the Power Transmitter and Power Receiver becomes important. Different shapes of the current limit yield a different trade-off between maximum load voltage and the coupling range.

Figure 15. System control at power-dependent maximum Primary Coil current (1)



As a final example, Figure 16 illustrates the full operating space that results from the power-dependent current limit; the trajectories that result if the Power Receiver scales its power back from its target to load powers of 10 W, 5 W, and 3 W; and the maximum voltages that result from coupling steps at these additional Operating Points. In most cases, the maximum voltage does not exceed 20 V (rms), and where it does exceed 20 V (rms) it is not by much.

Figure 16. System control at power dependent maximum Primary Coil current (2)



All practical Power Receiver implementations use a rectifier as part of the load circuit shown in [Figure 11](#) (see also [Section 3.2, Rectification circuit](#)). Moreover, most Power Receiver implementations include a capacitor directly after this rectifier to smoothen the ripple on the rectified voltage. In combination with a high load impedance (low load current), this smoothing capacitor typically charges to a level approaching the peak voltage that is present at the input to the rectifier. When determining the appropriate (power-dependent) current limit this effect should be taken into account.

Special care should be taken in designing Power Transmitters that use duty-cycle control (instead of frequency or voltage control), because the peak voltage in those designs can be substantially higher than the rms voltage that is used in the above examples. (The voltage waveform at the input to the rectifier resembles the waveform generated by the Power Transmitter's power source.)

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11 External Power Input (Informative)

11.1 Available power—Extended Power Profile only

To meet the recommended minimum system efficiency (see [Section 13.2, Power Transmitter efficiency](#)), the power supply of a Power Transmitter should be able to provide at least 20 W.

Once the Power Transmitter has completed the *negotiation* phase, and therefore has established a Power Transfer Contract, its power supply should not reduce the power below the level that is necessary to fulfill the Guaranteed Load Power in the Power Transfer Contract. Note that this provision typically is relevant only if multiple Power Transmitters share a single power supply. For example, if two Power Transmitters share a single 30 W power supply, only one of the two at a time can negotiate a Guaranteed Load Power of 15 W—which translates to an input power of 20 W or more. The other one then has to stick to a Guaranteed Load Power of 5 W—which translates to an input power of 7.5 W or more. In order to make this work reliably, some communication should be provided between the Power Transmitters and the power supply.

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12 Power Levels (Extended Power Profile only)

12.1 Potential Load Power

The Power Transmitter designs using the Extended Power Profile can support a Potential Load Power of up to 15 W. A Power Transmitter that is constructed according to one of these Power Transmitter designs can provide the amount of power that Test Power Receiver #MP1 needs to function at its intended Control Point. In particular, this means that if Test Power Receiver #MP1 is positioned appropriately relative to the Power Transmitter, it can provide

- 8 W of power at its output in configuration A if the Potential Load Power is ≥ 8 W;
- 15 W of power at its output in configuration B if the Potential Load Power is 15 W; and
- 12 W of power at its output in configuration C if the Potential Load Power is ≥ 12 W.

12.2 Light load

A Power Transmitter shall be able to continuously provide power at 5% of the Maximum Power level that is contained in the Power Transfer Contract, with a minimum of 250 mW.

NOTE: Power Receivers that operate in stand-by mode, or have a nearly full battery may present such a light load to the Power Transmitter for longer periods of time. The minimum light-load power level that a Power Transmitter is required to support corresponds to a negotiated Maximum Power level of 5 W.

13 System Efficiency (Informative)

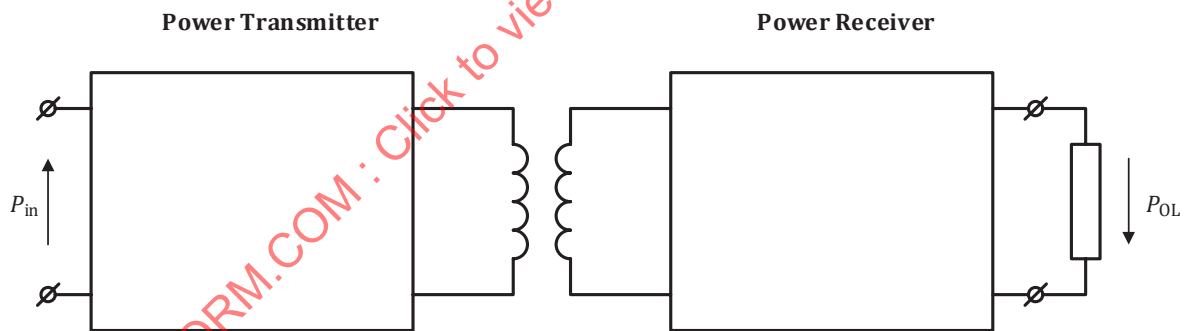
The efficiency of a wireless power transfer System depends on the combination of the specific Power Transmitter and the specific Power Receiver that are used, as well as their alignment. Since the Power Transmitter and Power Receiver are subsystems of two separate pieces of end equipment that may originate from different manufacturers, the efficiency of each can only be measured with a reference test fixture of the other subsystem. Below defines the procedure to measure the system efficiency with the help of the Test Power Transmitters and Test Power Receivers.

13.1 Definition

Figure 17 shows a schematic diagram of a wireless power transfer System, consisting of a Power Transmitter coupled to a Power Receiver. As illustrated, P_{in} represents the DC input power to the (inverter stage of the) Power Transmitter, and P_{OL} represents the amount of DC power that is consumed in the load that is connected to the output terminals of the Power Receiver. The system efficiency is defined as:

$$\eta_{\text{system}} = \frac{P_{OL}}{P_{in}}$$

Figure 17. System efficiency



13.2 Power Transmitter efficiency

13.2.1 Baseline Power Profile

Table 12 indicates the recommended minimum system efficiency of a Power Transmitter for Baseline Power Profile devices, as measured with the set of Test Power Receivers. It is also recommended that if the Power Transmitter Product is to be delivered with an AC adapter, the AC adapter should be Energy Star compliant.

Table 12: Recommended minimum system efficiency (Baseline Power Profile)

Test Power Receiver	Load [Ω]	Minimum System Efficiency [%]
TPR#1A	3.5	55
TPR#1B	8.7	65
TPR#1C	10	50
TPR#1D	75	25
TPR#1E	5	55

The system efficiency of the Power Transmitter Product is measured using Test Power Receiver #1. Measurement of the Power Transmitter efficiency shall proceed as follows:

1. Position Test Power Receiver #1 on the Interface Surface of the Power Transmitter Product.
2. Calculate the Power Transmitter efficiency η_{system} as:

$$\eta_{\text{system}} = \frac{P_{\text{OL}}}{P_{\text{in}}}$$

3. Repeat the above two steps 3 times, and calculate the average Power Transmitter efficiency η_{average} as:

$$\eta_{\text{average}} = \frac{1}{3} \sum_{i=1}^3 \eta_{\text{system}}(i)$$

13.2.2 Extended Power Profile

Table 13 provides recommendations for the minimum system efficiency for Extended Power Profile devices. Note that this table augments Table 12.

Table 13: Recommended minimum system efficiency (Extended Power Profile)

Test Power Receiver	Volume I Power Transmitter (5 W)		Volume II Power Transmitter (15 W)	
	Load [Ω]	Minimum System Efficiency [%]	Load [Ω]	Minimum System Efficiency [%]
TPR#1A	3.5	55	3.5	55
TPR#1B	8.7	65	8.7	65
TPR#1C	10	50	10	50
TPR#1D	75	25	75	25
TPR#1E	5	55	5	55
TPR#MP1A	—	—	4.2	65
TPR#MP1B	—	—	9.6	70
TPR#MP1C	—	—	12	75

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13.3 Power Receiver efficiency

Measurement of the Power Receiver efficiency shall proceed as follows:

1. **Baseline Power Profile:** Position the Power Receiver Product under test on the Interface Surface of Test Power Transmitter #2.
Extended Power Profile: Test Power Transmitter #MP1 is used to determine the efficiency of a Power Receiver that negotiates a Guaranteed Load Power Value of 15 W in the Power Contract.
2. The power delivered to the load of the Power Receiver must be predetermined or set to a known condition P_{OL} .
3. Measure the amount of power P_{in} input of the Test Power Transmitter, at a power dissipation P_{OL} in the load of the Power Receiver under test.
4. Calculate the system efficiency for the Power Receiver η_{system} as:

$$\eta_{system} = \frac{P_{OL}}{P_{in}}$$

5. Repeat the above 3 steps 3 times, and calculate the average Power Receiver efficiency $\eta_{average}$ as:

$$\eta_{average} = \frac{1}{3} \sum_{i=1}^3 \eta_{system}(i)$$

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